Embedded DC-DC Converters Using the ISL6431 PWM Controller ICs

Application Note | September 2001 | AN9975

Introduction

The ISL6431 is a voltage mode controller with many functions that are needed for a multitude of demanding applications. The ISL6431 a contains a high performance error amplifier, a high accuracy reference, a fixed 300kHz internal oscillator and over-current protection circuitry. There are two MOSFET drivers for use in synchronous-rectified buck converters. The ISL6431 is also capable of regulating the output voltage while the DC-DC converter is sinking current. All these features are packaged in a small, 8 pin SOIC. More complete descriptions of the ISL6431 can be found in the datasheets [1].

This application note details the ISL6431 in DC-DC converters for applications requiring a tightly regulated, fixed output voltage. Any low-cost application requiring a DC-DC converter can benefit from one of the designs presented in this application note.

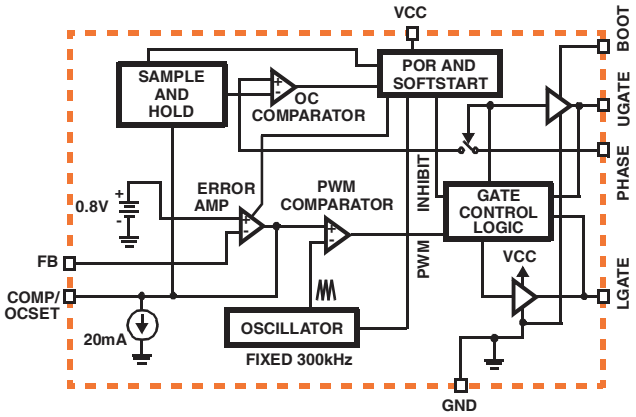


FIGURE 1. ISL6431 BLOCK DIAGRAM

ISL6431 Reference Design

The ISL6431EVAL1 is an evaluation board that highlights the operation of the ISL6431 in an embedded application. The ISL6431EVAL1 is flexible enough to allow for reference designs with 5A, 10A, and 15A output currents at a fixed output voltage of 3.3V. A simple resistor change allows the output to go as low as 0.8V, to as high as the input voltage. This flexibility allows a power supply designer to easily modify an existing design to suit almost any relevant application. The ISL6431EVAL1 DC-DC converter demo boards are customized to provide up to 15A of current at a fixed output voltage. The circuit configurations described in this application note refer to the demo board customized to 15A, unless otherwise noted. The schematic, Bill of Material, and Board Layout for the ISL6431EVAL1 can be found in the appendix. Customization of the reference design is discussed below.

Quick Start Evaluation

The input to the ISL6431EVAL1 board will only accept 5V from a standard power supply. The outputs can be exercised using either resistive or electronic loads. The shutdown switch, SW1, will allow the designer to evaluate how the ISL6431 shuts down and starts up. Pressing the switch will shut the converter down while releasing it will allow the converter to restart.

Startup

Figure 2 shows a typical startup sequence. Once the input voltage has exceeded the power-on reset (POR) threshold level, the IC will begin its start up sequence.

First, the error amplifier is disabled allowing 20µA of current to be drawn through a resistor tied between V_{CC} and the COMP/OCSET pin. The voltage that is impressed across the resistor is then read and sampled at the COMP/OCSET pin, with respect to V_{CC}. It is then held in internal memory as the overcurrent set point used in the upper MOSFET $R_{DS(ON)}$ overcurrent sensing feature.

After the overcurrent set point is established, the error amplifier is re-enabled and the ISL6431 then initiates its soft start sequence through the use of an internally generated soft start ramp. The entire start up procedure typically takes about 11ms from POR.

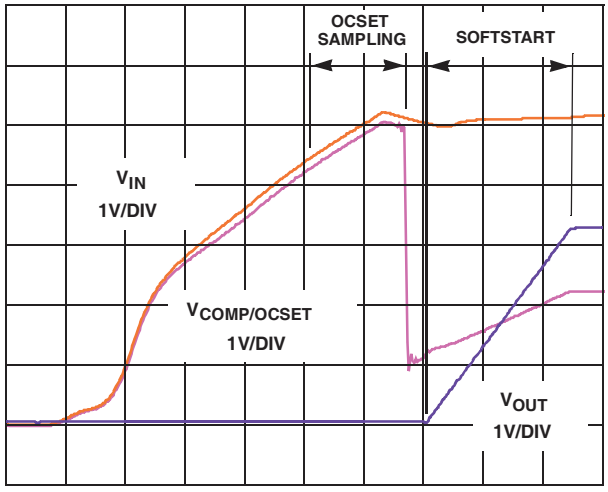


FIGURE 2. SYSTEM STARTUP

Shutdown and Restart

DC-DC converters that utilize the ISL6431 may be shut down by pulling the COMP/OSCET pin below 0.8V. One method to implement this feature is to connect the drain of a source-grounded small signal MOSFET to the

COMP/OSCET pin so that an external signal may trigger the command. The regulator will react to the shutdown command by pulling both of the MOSFET gates to ground, thus shutting down the converter.

The ISL6431EVAL1 board demonstrates the shutdown feature with a push button. Depressing the push button will disable the converter by pulling the COMP/OSCET pin to ground. Once released, the converter will follow its normal start up procedure, which includes the overcurrent set point programming and soft start.

Reference Design Customization

The ISL6431EVAL1 evaluation board was designed to be as flexible as possible for the power supply designer. The board will accommodate either DPAK or D2PAK packaged MOSFETs in the same footprint and in either the upper or lower MOSFET locations. This allows for a wide range of power levels on the same board. The designer may also implement either a Type II or a Type III compensation network. Finally, there are component locations in place that allow the designer to incorporate output voltage droop into the design.

Table 1 presents reference values for three different converter designs that may be used on the ISL6431EVAL1 board. The reference designs are optimized for 5A, 10A and 15A maximum output capabilities. For further customization, recommended guidelines for component selection are included below.

Input Capacitor Selection

The number of input capacitors and their capacitances are usually determined by their maximum RMS current ratings. A conservative approach to determining the number and type of input capacitors is to determine the converter maximum input RMS current and assume it would all be supplied by the input capacitors. This approach works well for converters that employ a filtering inductor on their inputs. In these types of converters, all of the RMS current is supplied by the input capacitors. For converters that do not employ an input inductor, such as the reference design on the ISL6431EVAL1 board, the conservative approach may be too costly. The number of capacitors may be decreased by assuming that only 50% of the RMS current is supplied by the input capacitors. This approach will usually provide enough capacitors to provide proper power decoupling.

The voltage rating at maximum ambient temperature should be 1.25–1.5 times the maximum input voltage. More conservative approaches can bring the voltage rating up to two times the maximum input voltage. High frequency decoupling, which is highly recommended, is implemented through the use of ceramic capacitors in parallel with the bulk capacitor filtering.

The reference design utilizes Sanyo 330µF, 6.3V POSCAP capacitors as the bulk input capacitors (Sanyo Part Number 6TPB330M). Each of these capacitors has a $3A_{RMS}$ maximum allowable ripple current rating. The number of capacitors used in each design, which is shown in Table 1, is more than sufficient to handle the input RMS current under the assumption that only 50% of that current is being supplied by the input capacitance.

MOSFET Selection

The ISL6431EVAL1 board can accommodate multiple MOSFET package styles. Each placeholder can accommodate DPAK or D2PAK package connections. The output loading and the thermal environment ultimately dictate the MOSFET selected. While many factors are involved in the selection of the MOSFETs, overall efficiency of the regulator should be a major contributor. There are three major aspects of power loss that are associated with the MOSFET. These are gate drive power losses, conduction losses and switching losses.

TABLE 1. ISL6431EVAL1 DESIGN RECOMMENDATIONS

COMPONENTS	REFERENCE DESIGN	MAXIMUM LOAD CURRENT		
		DESIGN A - 5A	DESIGN B - 10A	DESIGN C - 15A
MOSFETS	Q1, Q2	FAIRCHILD HUF76121D3S	FAIRCHILD HUF76129D3S	FAIRCHILD HUF76143S3S
Inductor	L1	6.4µH Panasonic ETQP6F6R4HFA	3.2µH Panasonic ETQP6F3R2HFA	2.0µH Panasonic ETQP6F2R0LFA
Number of Input Capacitors	C12, C13	1	1	2
Number of Output Capacitors	C8, C9, C10	1	2	3
Number of Decoupling Capacitors	C5A, C5B	1	1	2
OCSET Resistor	R5	9.06kΩ	12.7kΩ	6.34kΩ

Gate drive power losses result in the power dissipated within the gate drivers, which are located in the ISL6431. This power loss is a result of displacing the charge on the gate-to-source capacitance, C_{GS}.

The gate power is frequency dependent and is determined by the equation:

$$P_{gate} = (Q_{gu} x V_{gu} + Q_{gl} x V_{gl}) x F_s$$

where

Q_{gu} = Upper MOSFET gate charge

V_{gu} = Upper MOSFET gate voltage

Q_{gl} = Lower MOSFET gate charge

V_{gl} = Lower MOSFET gate voltage

Conduction losses are simply I^2R losses. Conduction losses (P_{CON}) can be approximated as:

$$P_{CON} = R_{DSU} x D x I_{LOAD}^2$$

$$P_{CON} = R_{DSL} x (1 - D) x I_{LOAD}^2$$

where

P_{CON} = Upper MOSFET Conduction Loss

P_{CON}= Lower MOSFET Conduction Loss

R_{DSU} = Upper MOSFET $R_{DS(ON)}$

R_{DSL} = Lower MOSFET $R_{DS(ON)}$

D = Duty Cycle

I_{LOAD}= Load Current

Note that the $R_{DS(ON)}$ will increase as the junction temperature of the MOSFET increases. This increase in impedance should be taken into account when calculating the conduction losses.

Switching losses are caused by crossover conduction during the switching interval and by the output capacitance, Coss, being displaced. Since the dissipation caused by the output capacitance is very small compared to the loss due to crossover conduction, it can be ignored.

The equations shown below give a simplified, yet useful, representation of switching loss for a MOSFET

$$P_{switch} = \frac{1}{2} x V_{in} x I_{in} x t_{sw} x f_s$$

where

V_{in} = Input Voltage

I_{in} = Input Current

t_{sw} = MOSFET switching time

f_s = Switching Frequency

ISL6431EVAL1 Efficiency

Figure 3 shows the efficiency of the ISL6431EVAL1 for all three design recommendations: 5A maximum load, 10A maximum load, and 15A maximum load respectively. As can be seen in the efficiency curves, the MOSFETs and other components were selected so as to keep a high efficiency throughout the load range of the converter.

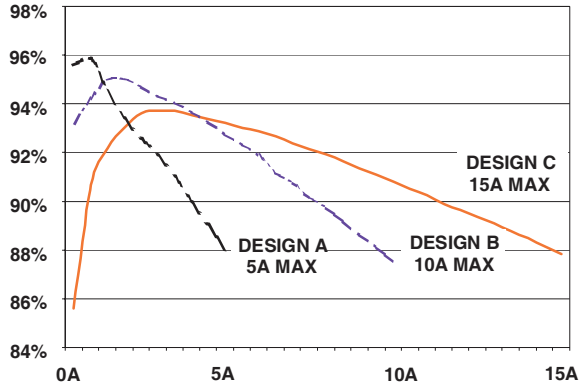


FIGURE 3. ISL6431EVAL1 EFFICIENCY

Output Voltage Programming

Simple resistor value changes allow for outputs as low as 0.8V or as high as the input voltage. The steady state DC output voltage can be set using the following formula:

$$V_{out} = V_{ref} x \left(1 + \frac{R1}{R4}\right)$$

where

V_{out} = Desired output voltage of converter

V_{ref} = ISL6431 internal reference (0.8V)

The output voltage of the reference designs presented in this application note is 3.3V.

Lossless Output Voltage Droop with Load

The ISL6431EVAL1 board has unpopulated component footprints in place to implement output voltage droop. Droop is an intentional sag in the output voltage that is proportional to the output current. Although not necessary for proper circuit operation, utilizing droop allows the dynamic regulation to be improved by taking advantage of static regulation requirements and expanding the available headroom for transient edge output excursions. In practical applications that are compared to a non-droop implementation, the droop implementation requires fewer output capacitors or better regulation with the same type and number of output capacitors.

By moving the regulation point ahead of the output inductor (at the PHASE node), droop becomes equal to the average voltage drop across the output inductor's DC resistance as well as any distributed resistance. The droop circuitry is simply an RC low pass filter placed across the output inductor. This filter must have the same time constant that

the output inductor and its corresponding DCR have. The design must be careful to include any parasitic impedances of the PC board if the DCR of the inductor is very low.

On the ISL6431EVAL1 board, this filter is represented by resistors R6 and R7 and capacitor C7. Resistor R7 can be used to scale the magnitude of the droop. The output of this low pass filter is fed directly into the feedback compensation network of the regulator. The effects of this filter on the frequency response of the converter is minimal and can be ignored when evaluating the frequency response of the converter. To insure symmetric output voltage excursions about the set voltage in response to load transients, the output voltage should be programmed to be above the nominal level by half the calculated droop.

As supplied, the ISL6431EVAL1 does not employ droop. A successful droop implementation has been designed and tested for Design C. The DCR of the output inductor is 5mΩ. This gives a time constant of:

$$\tau = \frac{L_{OUT}}{DCR + R_{PARASITIC}} = 400\mu S \qquad \text{with } R_{PARASITIC} = 0\Omega$$

The impedance portion of the time constant calculation for the RC filter includes the parallel combination of the filter resistor, R6, and the feedback resistor, R1. A value for R6 is chosen that will not significantly decrease the impedance already set by R1. A 16.2kΩ resistor was chosen. This yields an effective impedance of 2.64kΩ. The filter capacitor, C7, is then calculated:

$$\tau = RxC = 2644xC = 400\mu S$$

$$C \sim 0.1\mu F$$

Since the regulation point is now located at the phase node, and a 16.2kΩ resistor is being added to the DC path for regulation, then the resistor, R4, used to program the output voltage must be adjusted. The maximum output current for Design C is 15A and the DCR of the inductor is 5mΩ. This combination will yield a total droop of 75mV. In order to center the droop symmetrically about the 3.3V set point, the no load set point will be 3.375V. The corresponding value for R4 to accomplish this is 6.04kΩ.

Figure 4shows the output voltage of the converter with the droop circuitry added.

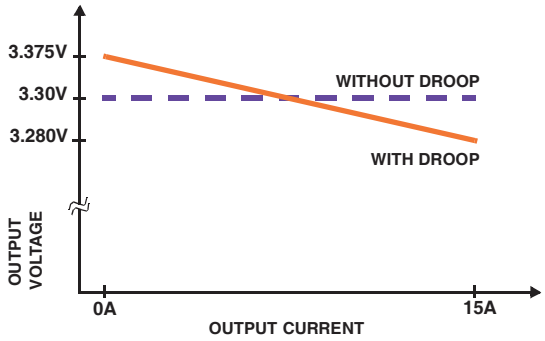


FIGURE 4. OUTPUT VOLTAGE DROOP

Component Values for Droop Implementation:

R6 = 16.2kΩ
R7 = Not Populated
C7 = 0.1μF
R4 = 6.04kΩ

With the proper selection of the components used in the RC filter actoss the inductor, the frequency response of the system is only minimally affected and the compensation network does not need to be recalculated.

Output Capacitor Selection

The shape of the output voltage waveform during a load transient that represents the worst case loading conditions will ultimately determine the number of output capacitors and their type. When this load transient is applied to the converter, most of the energy required by the load is initially delivered from the output capacitors. This is due to the finite amount of time required for the inductor current to slew up to the level of the output current required by the load. This phenomenon results in a temporary dip in the output voltage. At the very edge of the transient, the equivalent series inductance (ESL) of each capacitor induces a spike that adds on top of the existing voltage drop due to the equivalent series resistance (ESR)

After the initial spike, attributable to the ESR and ESL of the capacitors, the output voltage experiences sag. This sag is a direct consequence of the amount of capacitance on the output.

During the removal of the same output load, the energy stored in the inductor is dumped into the output capacitors. This energy dumping creates a temporary hump in the output voltage. The hump, as with the sag, can be attributed to the total amount of capacitance on the output.

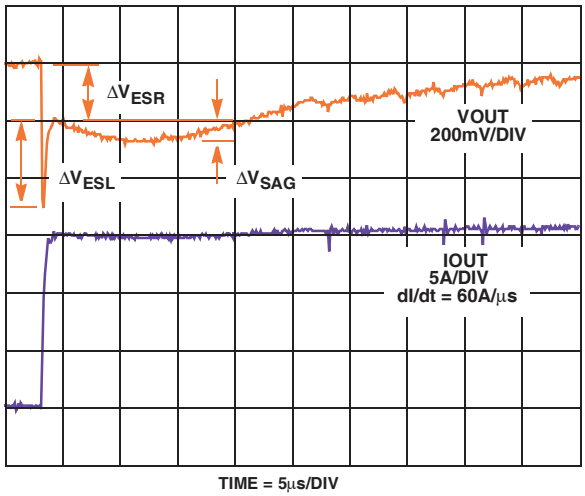


FIGURE 5. TRANSIENT RESPONSE

Figure 5 shows a typical response of the ISL6431EVAL1 to a load transient. The current slew rate was made large to show the effects of the parasitic inductances in the output stage.

The amplitudes of the different types of voltage excursions can be approximated by using the following formulae

$$\Delta V_{ESR} = ESR \times I_{tran} \qquad \Delta V_{ESL} = ESL \times \frac{dI_{tran}}{dt}$$

$$\Delta V_{SAG} = \frac{L_{out} \times I_{tran}^{2}}{C_{out} \times (V_{in} - V_{out})}$$

$$\Delta V_{HUMP} = \frac{L_{out} \times I_{tran}^{2}}{C_{out} \times V_{out}}$$

where

I_{tran} = output load current transient

C_{out} = total output capacitance

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. The ESR and the ESL are typically the major contributing factors in determining the output capacitance. The number of output capacitors can be determined by using the following equation that relates the ESR and ESL of the capacitors to the transient load step and the voltage limit (ΔVo):

$$\text{Number of Caps} = \frac{\frac{ESL \times \Delta I_{tran}}{dt} + ESR \times I_{tran}}{\Delta V_o}$$

If ΔVsag and/or ΔVhump are found to be too large for the output voltage limits, then the amount of capacitance may need to be increased. In this situation, a trade off between output inductance and output capacitance may be necessary.

The ESL of the capacitors, which is an important parameter in the above equations, is not usually listed in databooks. Practically, it can be approximated if an impedance vs. frequency curve is given for a specific capacitor:

$$ESL = \frac{1}{C} \times (2 \times \pi \times f_{res})^{2}$$

where f_{res} is the frequency where the lowest impedance is achieved (resonant frequency).

The ESL of the capacitors becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

Output Voltage Ripple

The amount of ripple voltage on the output of the DC-DC converter varies with the input voltage, switching frequency, output inductor, and output capacitors. For a fixed switching frequency and output filter, the voltage ripple increases with the input voltage. The ripple content of the output voltage can be estimated with the following equation:

$$\Delta V_{out} = \Delta I_L \times ESR$$

where

$$\Delta I_L = \frac{(V_{in} - V_{out}) \times \frac{V_{out}}{V_{in}}}{L_{out} \times f_s}$$

If the output capacitors have already been selected to meet certain transient requirements, then the ripple voltage can be set by the output inductance.

Figure 6 shows the output ripple for Design C.

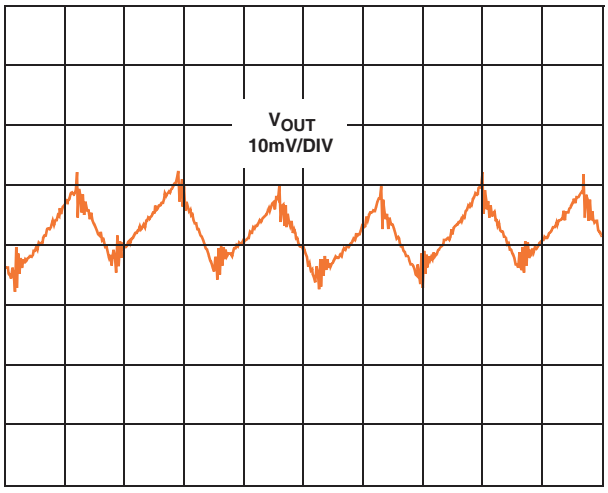


FIGURE 6. OUTPUT VOLTAGE RIPPLE

Conclusion

The ISL6431EVAL1 board is a DC-DC converter reference design that is flexible enough to accommodate a wide range of output current requirements. The printed circuit board is laid out to accommodate the necessary components for operation from low-load levels to 15A of output current.

References

For Intersil documents available on the web, see www.intersil.com/

[1] *ISL6431 Data Sheet,* Intersil Corporation, Doc. # 9018

ISL6431EVAL1 Schematic

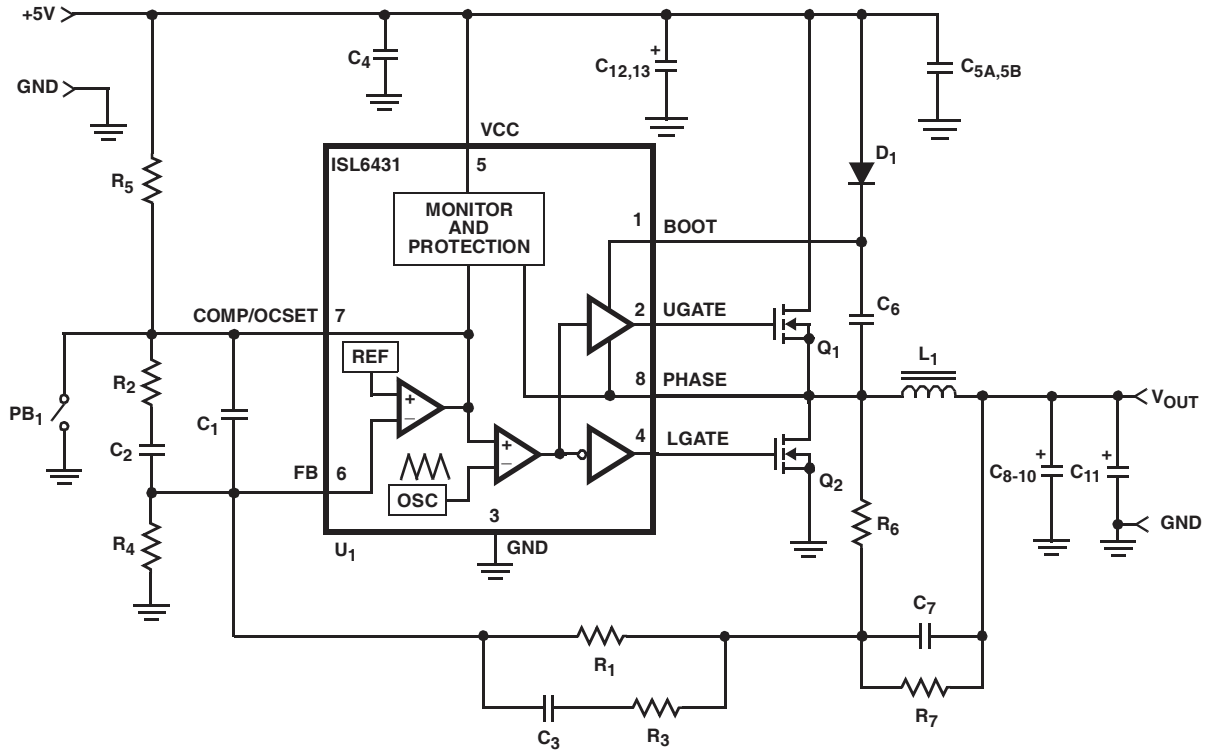
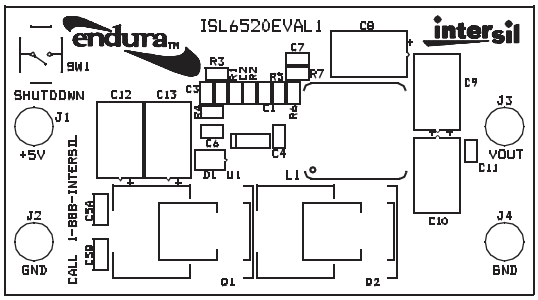


TABLE 2. ISL6431EVAL1 BILL OF MATERIAL

REF DES	DESCRIPTION	VENDOR	VENDOR P/N	QTY
C1	470pF Capacitor, 0603	Various	---	1
C2	8200pF Capacitor, 0603	Various	---	1
C3	18000pF Capacitor, 0603	Various	---	1
C4,C6,C11	0.1µF Capacitor, 0603	Various	---	2
C5A,C5B	1µF Capacitor, 0805	Various	---	2
C7	Not Populated Capacitor, 0603	---	---	---
C8-10, C12, C13	330µF Capacitor	Sanyo	6TPB330M	5
D1	Diode, 30mA, 30V	Digikey	MA732	1
L1	2µH Inductor	Panasonic	ETQP6F2ROLFH	1
Q1, Q2	MOSFET	Fairchild	HUF76143S3S	2
R1	3.16kΩ 1% Resistor, 0603	Various	---	1
R2	10.0kΩ 1% Resistor, 0603	Various	---	1
R3	60.4Ω 1% Resistor, 0603	Various	---	1
R4	1.00kΩ Resistor, 0603	Various	---	1
R5	6.34kΩ Resistor, 0603	Various	---	1
R6	Not Populated Resistor, 0603	---	---	---
R7	0Ω Resistor, 0603	Various	---	1
PB1	Pushbutton, miniature	Digikey	P8007S-ND	1
U1	Single Synchronous Buck PWM Controller	Intersil	ISL6431CB	1
TP1,2,3,4	Test Points	Keystone	1514-2	4

Board Description

Silk Screen



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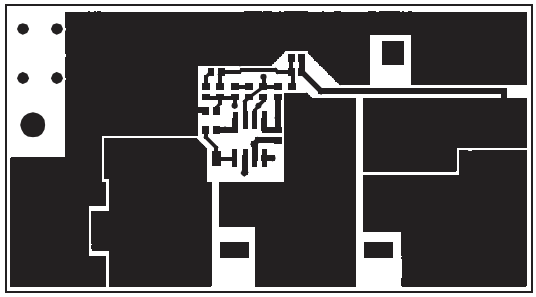
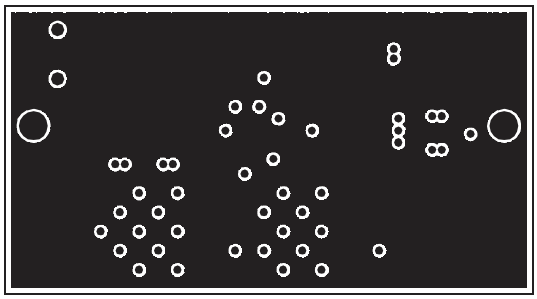
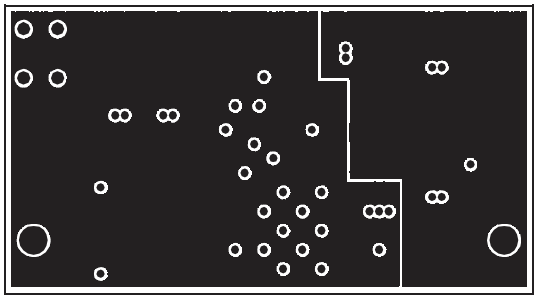


Ground Layer



Power Layer



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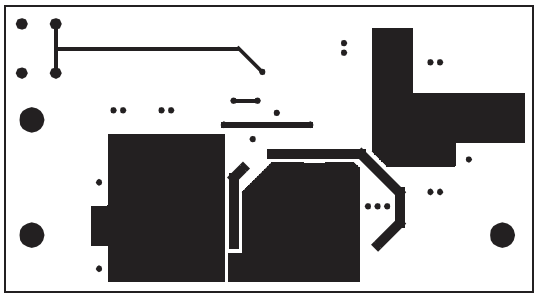

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